Remarks

The above Amendments and these Remarks are in reply to the outstanding Office Action. Claims 1-3, 5-8, 10-24, and 30 are currently pending. Claims 10-11, 14-24 and 30[1] are allowable.

Claims 2-3 and 7-8 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Claims 1, 5-6 and 13 are rejected under 35 U.S.C. §103(a) as being unpatentable over previously cited U.S. Patent No. 5,572,558 (*Beherns*) in view of newly cited U.S. Patent No. 6,285,228 (*Heyne, et al.*) and U.S. Patent No. 5,592,109 (*Notani, et al.*).

Claim 12 is rejected under 35 U.S.C. §103(a) as being unpatentable over *Beherns* in view of *Heyne, et al.* and *Notani, et al.* and further in view of previously cited U.S. Publication No. 20020030522 (*Nakamura*).

I. Rejection of Claims 1, 5-6 and 13 under 35 U.S.C. §103(a)

Claims 1, 5-6 and 13 are rejected under 35 U.S.C. §103(a) as being unpatentable over previously cited *Beherns* in view of *Heyne, et al.* and *Notani, et al.*

In rejecting independent claim 1, the Office Action at pages 3-4 states:

> Beherns discloses…a clock circuit (Fig. 3, unit 28) capable of generating a clock signal in response to a phase signal (VFO F50 provides a clock signal to the sampling device 24 based on error signal provided by the phase and frequency error detectors F54 and F52)…
>
> Thus [Beherns] discloses all the limitations, but fails to explicitly disclose whether the phase step size is adjustable…
>
> However, Heyne discloses a circuit comprising a clock circuit capable of generating a clock signal in response to an adjustable phase-step size (Column 2, lines 19-50; Fig. 4 and column 6, line 64-column 7, line 25. The phase regulator connected downstream of the phase detector generates an adjustable delay step using fine and course control signals and this is equivalent to claimed phase adjustable-step size). It would have been obvious to a person of ordinary skill in the art to use adjustable phase step in a clock circuit as shown by Heyne because this allows for more accurate generation of clock signal.
>
> Further, Notani discloses a clock circuit which includes at least four stages each having a respective stage output (Fig. 6 and 16…)
>
> Thus, it would have been obvious to a person of ordinary skill in the art to use the four stage structure in the clock circuit as disclosed by Notani because Notani's

[1] While the "Office Action Summary" lists claim 30 as rejected, the "Detailed Action" at page 8 identifies claim 30 as allowed and there is not a detailed rejection of claim 30 in the "Detailed Action" of the Office Action. Accordingly, the Applicant believes that the Examiner intended to identify claim 30 as allowable in the "Office Action Summary" and has responded accordingly. Clarification is respectfully requested if claim 30 is not allowable.

technique performs phase comparison at high speed with a simple structure and facilitates stability (Column 15, lines 43-54)

The Applicant's attorney respectfully disagrees that it would be obvious to one of ordinary skill in the art to combine the circuits of *Heyne* and *Notani, et al.* with *Beherns*. The circuits in these references solve different problems and operate substantially differently from each other. For example, it is not obvious to a person of ordinary skill in the art how *Heyne* and *Notani, et al.* can be reasonably combined to generate an operable circuit. If the Examiner is thinking about replacing the phase comparator $\Delta\phi$ in FIG. 4 of *Heyne* with phase comparator of FIG. 6 in *Notani, et al.*, the resulting circuit will not work or work any better than the original circuits. Note that the *Notani, et al.* phase comparator in FIG. 6 generates two outputs (up and down) that are each "1" or "0" (*Notani, et al.*, col. 21, lines 1-45). So, there are four possible combinations of these two outputs, which are sufficient for the phase regulator C in FIG 4 of *Heyne* to form the eight bits of a digital control word, A0 to A7, so as to facilitate coarse and fine control of the phase of the output signal (*Heyne*, col. 7, lines 3-15). So, a person of ordinary skill in the art would not be reasonably motivated to combine *Notani, et al.* with *Heyne*.

Further, the Office Action has not met its burden of establishing a prima facie case of obviousness by pointing out that all elements of the claims, such as claim 1, is taught or suggested in the cited references. For example, the Office Action has not identified with specificity the claimed "stall logic capable of holding the third and fourth stage outputs..." The Office Action has not identified a reference numeral in Figs. 6 or 16 or elsewhere in *Notani, et al.* that corresponds to the claimed "stall logic..."

Claims 5-6 and 13 depend from claim 1 and therefore are patentable for at least the reasons stated above in regard to claim 1.

It is therefore respectfully requested that the rejection of claims 1, 5-6 and 13 under 35 U.S.C. §103(a) be withdrawn.

II. Rejection of Claim 12 under 35 U.S.C. §103(a)

Claim 12 is rejected under 35 U.S.C. §103(a) as being unpatentable over *Beherns* in view of *Heyne* and *Notani, et al.* and further in view of previously cited *Nakamura*.

Claim 12 depends from claim 1 and therefore is patentable for at least the reasons stated above in regard to claim 1.

Therefore, it is respectfully requested that the rejection of claim 12 under 35 U.S.C. §103(a) be withdrawn.

III. Conclusion

Based on the above amendments and these remarks, reconsideration of claims 1-3, 5-8, 10-24, and 30 is respectfully requested.

The Examiner's prompt attention to this matter is greatly appreciated. Should further questions remain, the Examiner is invited to contact the undersigned attorney by telephone.

The Commissioner is authorized to charge any underpayment or credit any overpayment to Deposit Account No. 501826 for any matter in connection with this response, including any fee for extension of time, which may be required.

Respectfully submitted,

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